PersonalTech
For A Better World

JPX PRIME

[Provisional Translation Only]
This English translation of the original Japanese document is provided solely for information purposes. Should there be any discrepancies between this translation and the Japanese original, the latter shall prevail.

February 12, 2025

Japan Display Inc. (JDI) (Tokyo Stock Exchange Prime Market, 6740)
Representative: Scott Callon, Chairman, CEO
Inquiries: Ken Hirabayashi, CFO
Telephone: +81-3-6732-8100
www.j-display.com/en/

Strategic Alliance with TECH EXTENSION, Global Leader in Next-Generation 3D Semiconductor Integration Technology
– Launching BBCube 3D Semiconductor Integration Line at JDI Ishikawa Fab –

JDI has signed an equity investment agreement and a strategic alliance MOU with TECH EXTENSION Co. Ltd. (TEX), the global leader in next-generation 3D semiconductor integration technology spun out of the WOW Alliance[i] at Science Tokyo (Tokyo University of Science, formerly Tokyo Institute of Technology). The strategic alliance will facilitate the launch of a manufacturing line at JDI's Ishikawa Fab deploying next-generation 3D semiconductor integration based on TEX's world-leading BBCube (Bumpless Build Cube)[ii] technology.

1. Alliance Background and Purpose

In line with its BEYOND DISPLAY growth strategy announced on November 13, 2024, JDI is working to grow its advanced semiconductor packaging business into a significant growth driver. By partnering with TEX, the global leader in next-generation 3D semiconductor integration technology, JDI is creating a powerfully integrated and streamlined semiconductor supply chain at its Ishikawa Fab spanning production to sales.

2. Alliance Overview

JDI and TEX have agreed to establish a next-generation 3D integration manufacturing line at JDI's Ishikawa Fab, leveraging TEX's deep-tech BBCube technology, and have initiated discussions on forming a new company to deliver this technology rapidly and at scale . To further solidify their partnership, JDI is making an equity investment in TEX. JDI and TEX will implement the world's first integrated manufacturing line for next-generation 3D integration based on BBCube technology, using JDI's Ishikawa Fab for the entire process – from Wafer on Wafer (WOW)[iii] to Panel Level Packaging (PLP)[iv] – significantly progressing the deployment and social use of next-generation 3D integration technology[v] in the post-miniaturization era.

TEX will transfer WOW and Chip on Wafer (COW)[vi] technologies, key components of BBCube technology, to the Ishikawa Fab. This tech transfer will leverage the process technology, equipment, and materials developed by the WOW Alliance.

As invisible defects at the atomic level increase and yield rates stagnate, the importance of WOW stacking technology and COW horizontal and vertical chiplet integration grows. The alliance addresses these issues, linking product-out and market-in strategies and strengthening the global semiconductor supply chain. The new Ishikawa Fab 3D integration manufacturing line is scheduled for launch in the second half of 2025, with WOW and COW technologies being implemented sequentially. Furthermore, the alliance will engage

in research and development, including human resource development, in partnership with the Science Tokyo WOW Alliance, other universities, and industry stakeholders.

3. TEX Overview

(1) Name	TECH EXTENSION Co., Ltd.	
(2) Headquarters	3-15-9 Okamoto, Setagaya-ku, Tokyo 157-0076	
(3) Representative	Tadashi Fukuda, President	
(4) Business Description	Research and development of 3D structured LSIs, licensing of intellectual property, consulting, and technical support	
(5) Date of Incorporation	January 16, 2018	
(6) Relationship with JDI	Capital Relationship	N/A
	Personnel Relationship	N/A
	Business Relationship	N/A

4. Earnings Impact

The impact of this strategic alliance on FY25/3 earnings is expected to be minor, but JDI believes it will be a significant earnings and value driver over time.

---

[i] **Science Tokyo Comprehensive Research Institute WOW Alliance Heterogeneous Function Integration Research Unit** (formerly Tokyo Institute of Technology Science and Technology Creation Research Institute Heterogeneous Function Integration Research Unit). This is an industry-academia research platform led by Specially Appointed Professor Takayuki Ohba. It consists of companies and research institutions involved in semiconductor-related design, processes, equipment, and materials. As the only domestic entity conducting demonstration development using 300mm wafers for three-dimensional development, it possesses advanced and simple wafer thinning and stacking technologies, and was the first in the world to successfully develop three-dimensional technology using bumpless TSV wiring.

[ii] **BBCube Technology**: This architecture allows for compact three-dimensional integration of chips without using bumps, enabling system miniaturization and achieving 1/1000th the power consumption compared to conventional systems.
Reference: Ohba, T.; Sakui, K.; Sugatani, S.; Ryoson, H.; Chujo, N. Review of Bumpless Build Cube (BBCube) Using Wafer-on-Wafer (WOW) and Chip-on-Wafer (COW) for Tera-Scale Three-Dimensional Integration (3DI). Electronics 2022, 11, 236

[iii] **Wafer-on-Wafer (WOW) Technology**: A stacking technology that connects and stacks multiple wafers while bonding them on top of each other. This significantly contributes to productivity improvement in wafer stacking of identical chip sizes, such as DRAM.

[iv] **Panel Level Package (PLP)**: An application of the concept of batch manufacturing of chips, adopted in FOWLP (Fan Out Wafer Level Package), to panel-level manufacturing.

[v] **Next-Generation 3D Integration Technology**: A next-generation semiconductor technology that performs three-dimensional integration at the wafer level. Utilizing ultra-thin technology and vertical wiring technology without bumps owned by the WOW Alliance, it achieves higher performance and lower power consumption than conventional methods. It also enables the miniaturization of heterogeneous function device systems, not only for large-scale computing devices like servers.

[vi] **Chip-on-Wafer (COW) Technology**: A technology that connects and stacks chiplets on a wafer using WOW technology. By bonding chips onto the wafer, high-precision processing can be performed in subsequent semiconductor manufacturing processes using various wafer process equipment.