



[Provisional Translation Only]

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**Exhibition of Advanced Semiconductor Packaging Substrates at JPCA Show 2025
– Showcasing JDI’s Ultra-Fine RDL on Ceramic Substrates Using World-Class
Glass Substrate Processing Technology –**

In collaboration with PanelSemi Corporation (Taiwan), a pioneer in advanced semiconductor packaging technologies, JDI is exhibiting its ultra-fine redistribution layer (RDL) on ceramic substrate technology at the upcoming JPCA Show 2025 (June 4–6 at Tokyo Big Sight).

With the rapid expansion of generative AI, 5G, and high-performance computing (HPC), more advanced semiconductor packages are required to deliver high density and high integration, low power consumption, high bandwidth and high-speed data transfer, and dimensional stability. As a result, there is growing demand for high-performance substrates made from new materials such as glass and ceramics, which can overcome the limitations of conventional organic substrates in achieving fine-pitch wiring, dimensional stability, and thermal expansion control. In particular, technologies that enable fine-pitch RDL are becoming a key part of advanced semiconductor packaging.

Leveraging its world-class ultra-fine processing technology developed over many years in the field of glass substrates, JDI has successfully formed fine-pitch RDL on ceramic substrates. This technology enables high-density, highly integrated, and multifunctional packaging by utilizing ceramic core substrates.

Fine-pitch RDL allows for line widths and spacing to be reduced to the micrometer level, enabling multiple chips to be placed in close proximity. This contributes to reduced signal delay and lower power consumption. Additionally, the increased design flexibility supports complex chip configurations, further enhancing the functionality of advanced semiconductor packages.

Using ceramic as the substrate material significantly reduces warping compared to conventional organic substrates and greatly mitigates issues related to thermal expansion and heat dissipation. Notably, the coefficient of thermal expansion (CTE) of ceramics is close to that of silicon, minimizing thermal mismatch with chips and enabling highly reliable packaging by reducing mechanical stress.

Through this joint exhibition, JDI and PanelSemi aim to showcase the potential of substrate technologies that meet the high functionality demands of advanced semiconductor packaging and contribute to the further development of the global semiconductor industry.

JPCA Show 2025

Venue: Tokyo Big Sight, East Hall 5 (Booth No.: 5C12)

Dates: June 4–6, 2025

<https://www.jpcahow.com/show2025/en/index.html>